In the Specification:

Please replace replace the first paragraph of the Summary of the Invention, lines 15 – 25 on page 3 and lines 1 and 2 on page 4 with the following paragraph:

In accordance with the present invention, at least one column of a latch array includes a tri-state buffer in the upper portion of the column that receives the output of the uppermost latch of the column as its input, and which is enabled ~~and which is enabled~~ by a dump signal when a latch in the upper portion is addressed. When the dump signal that triggers the tri-state buffer is asserted, whatever is at the input of the tri-state buffer is driven by the buffer to the bottom of the latch array column, thereby providing the driven signal with sufficient strength to obviate transition timing and signal integrity problems. When the dump signal that triggers the tri-state buffer is not asserted, the tri-state buffer output exhibits high impedance, which isolates the lower portion of the latch array column from the upper portion of the latch array column, thereby preventing the capacitance associated with the line connecting the tri-state buffer to the output of the uppermost latch from affecting the driving ability of the latches in the lower portion of the column.